

FIG. 1

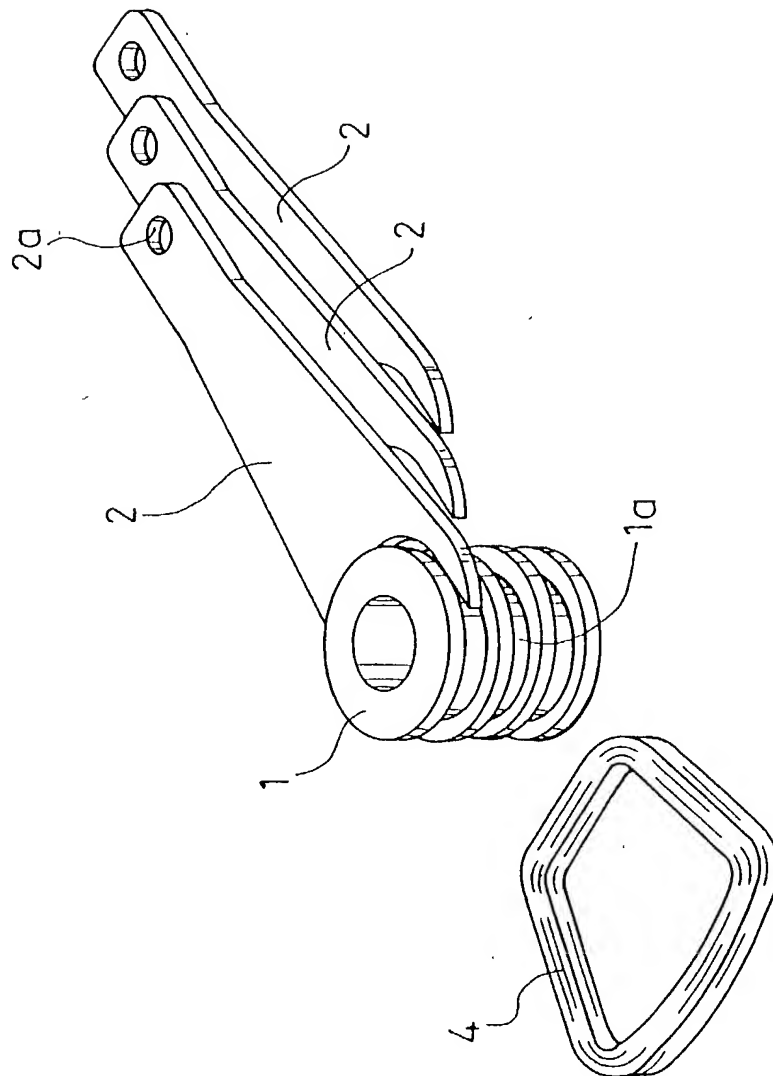


FIG. 2

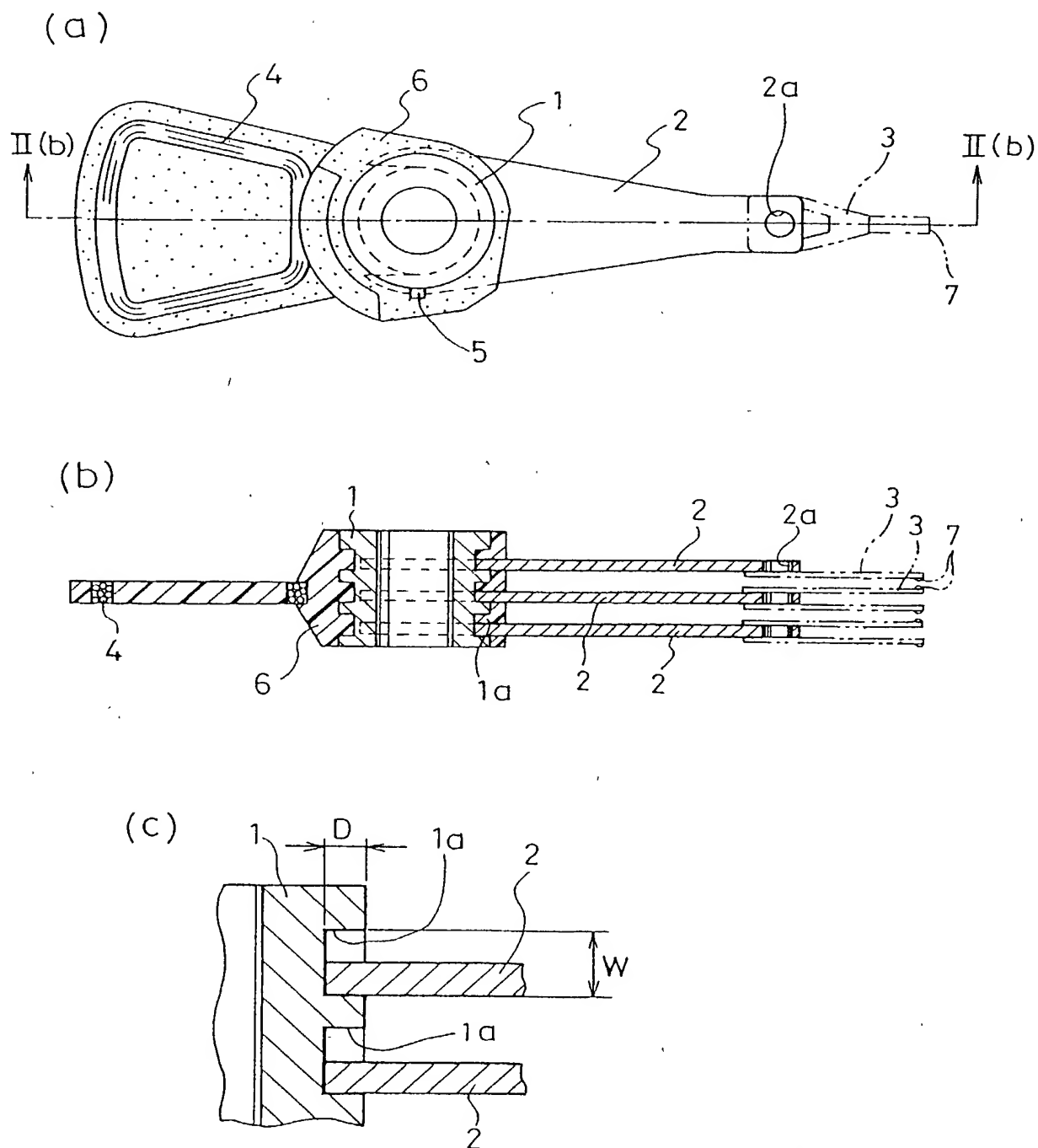


FIG. 3

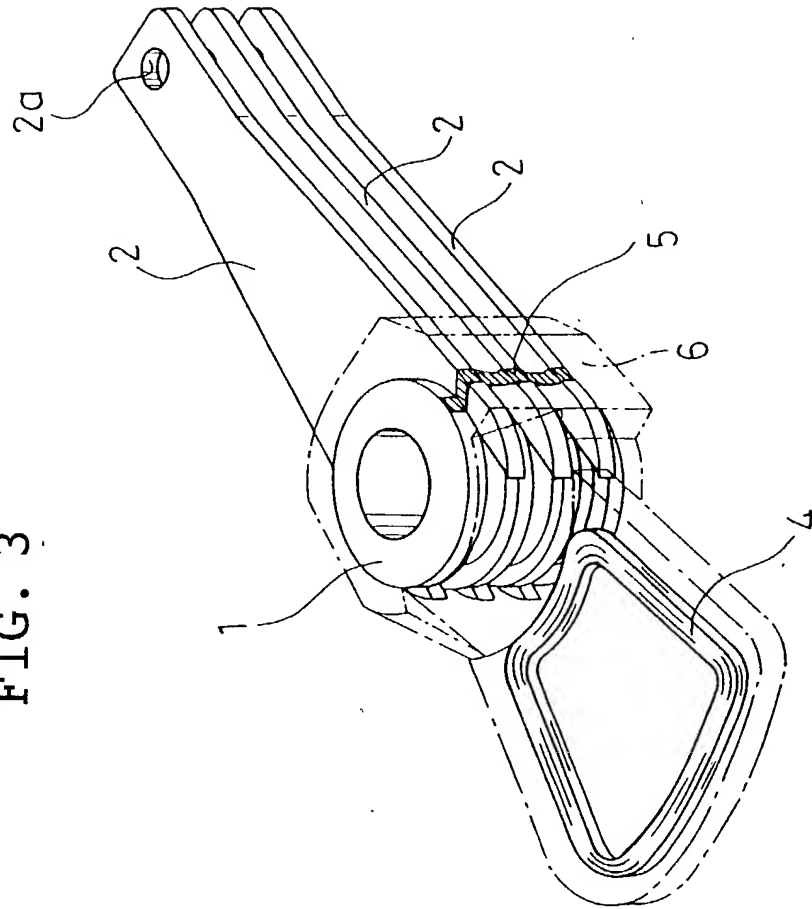


FIG. 4

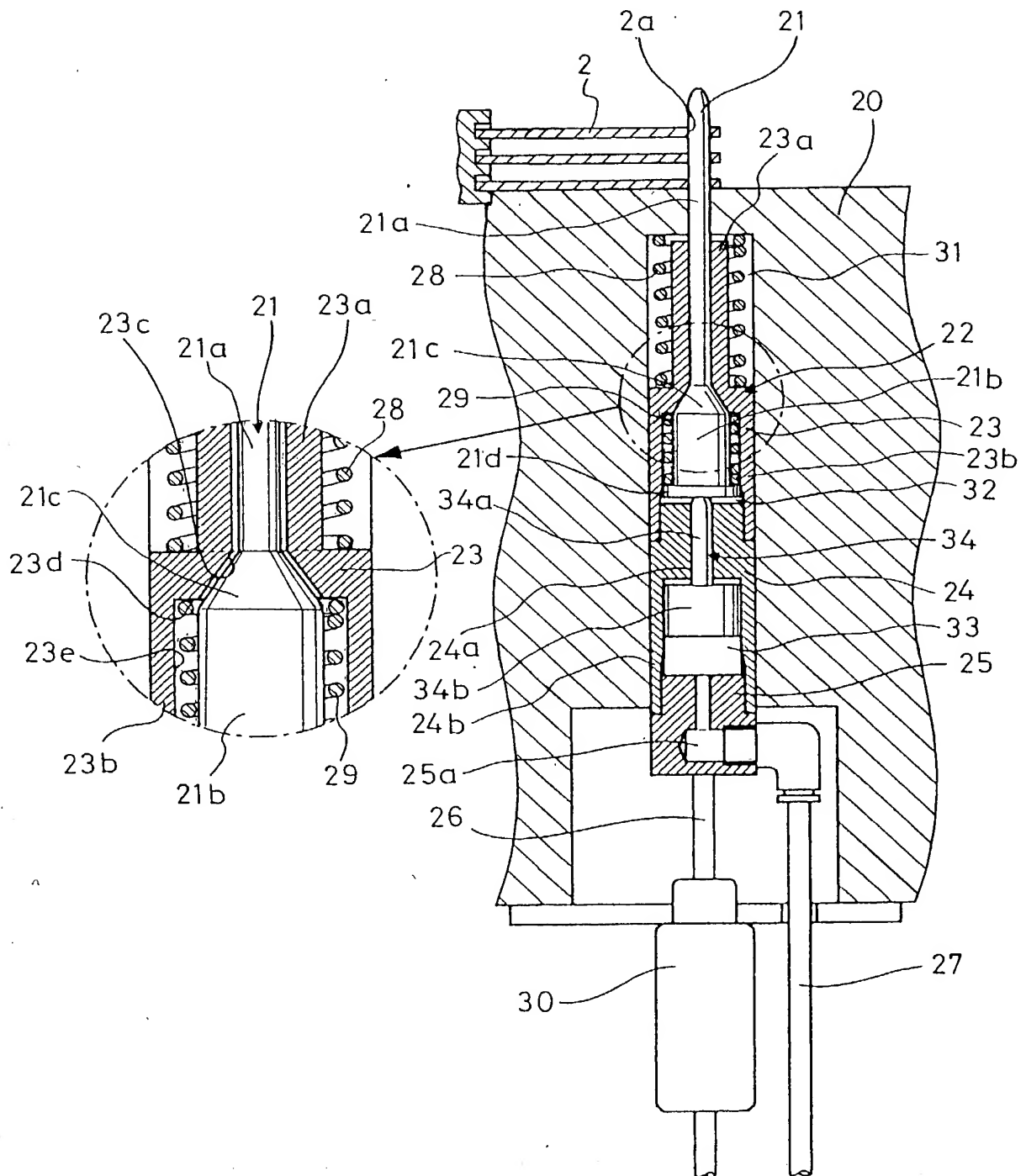


FIG. 5

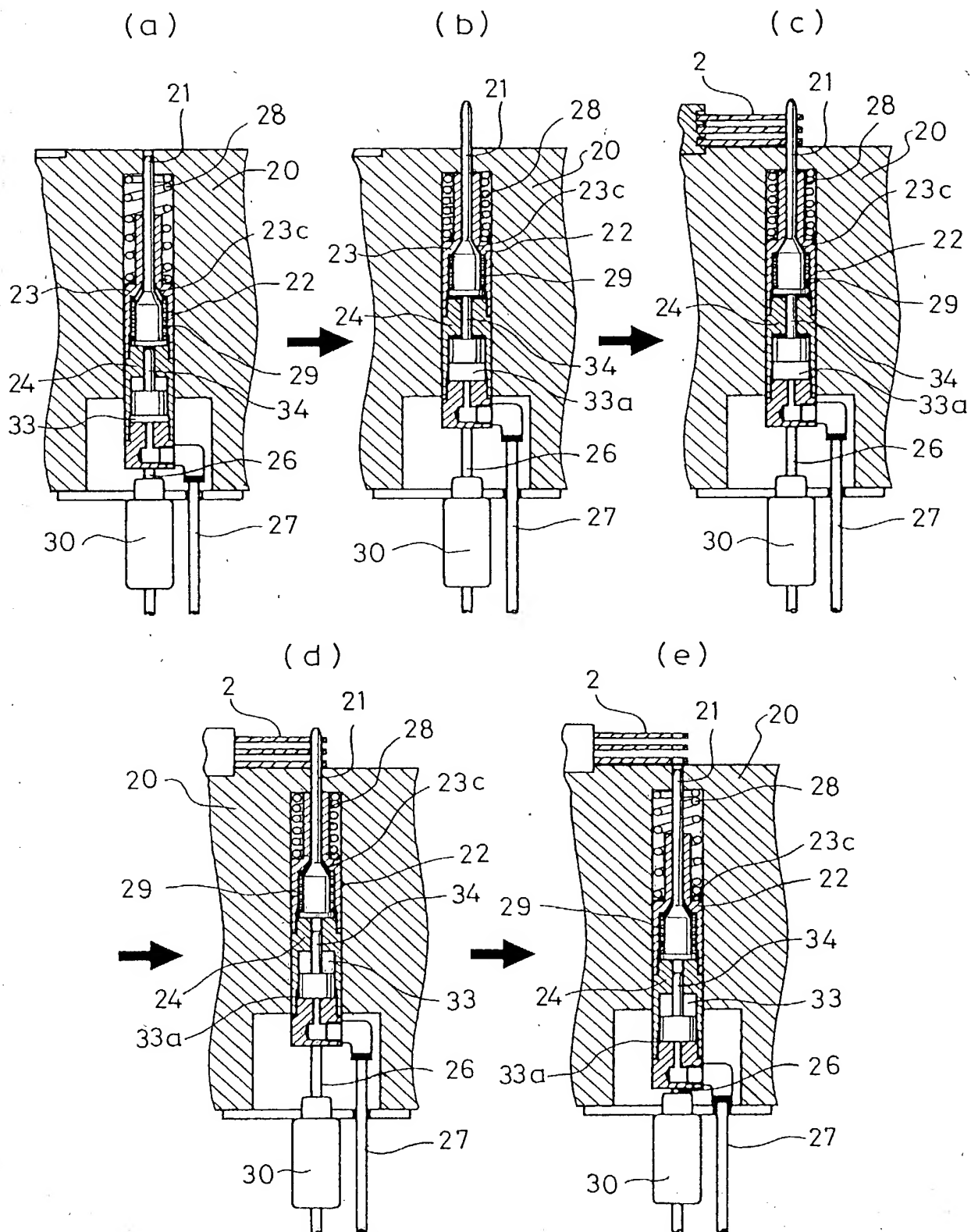
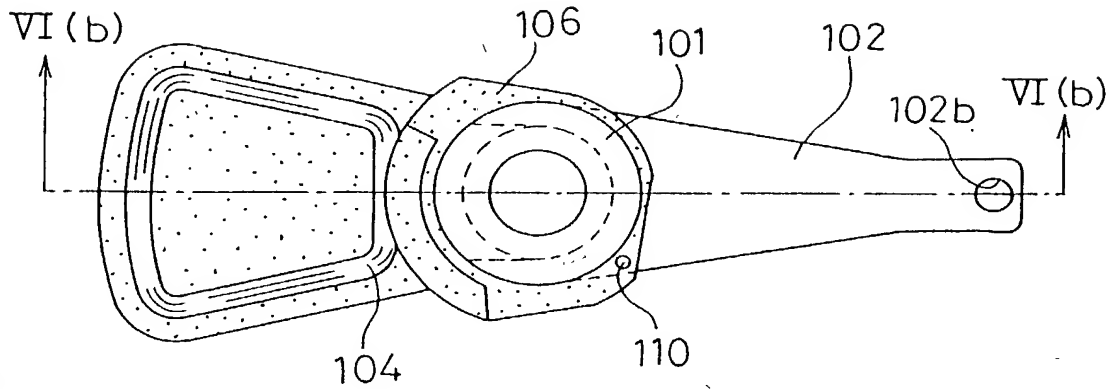


FIG. 6

(a)



(b)

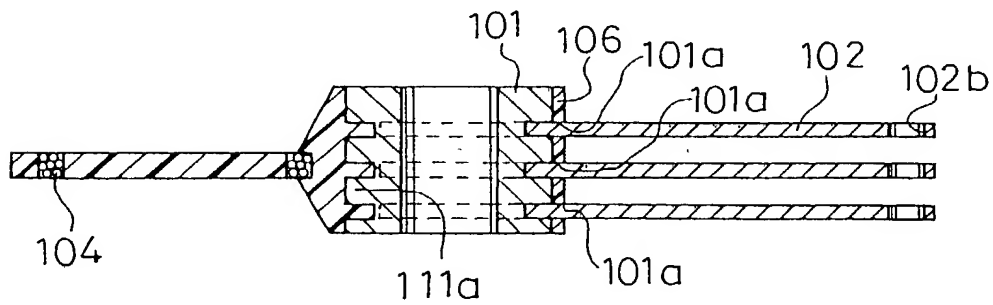


FIG. 7

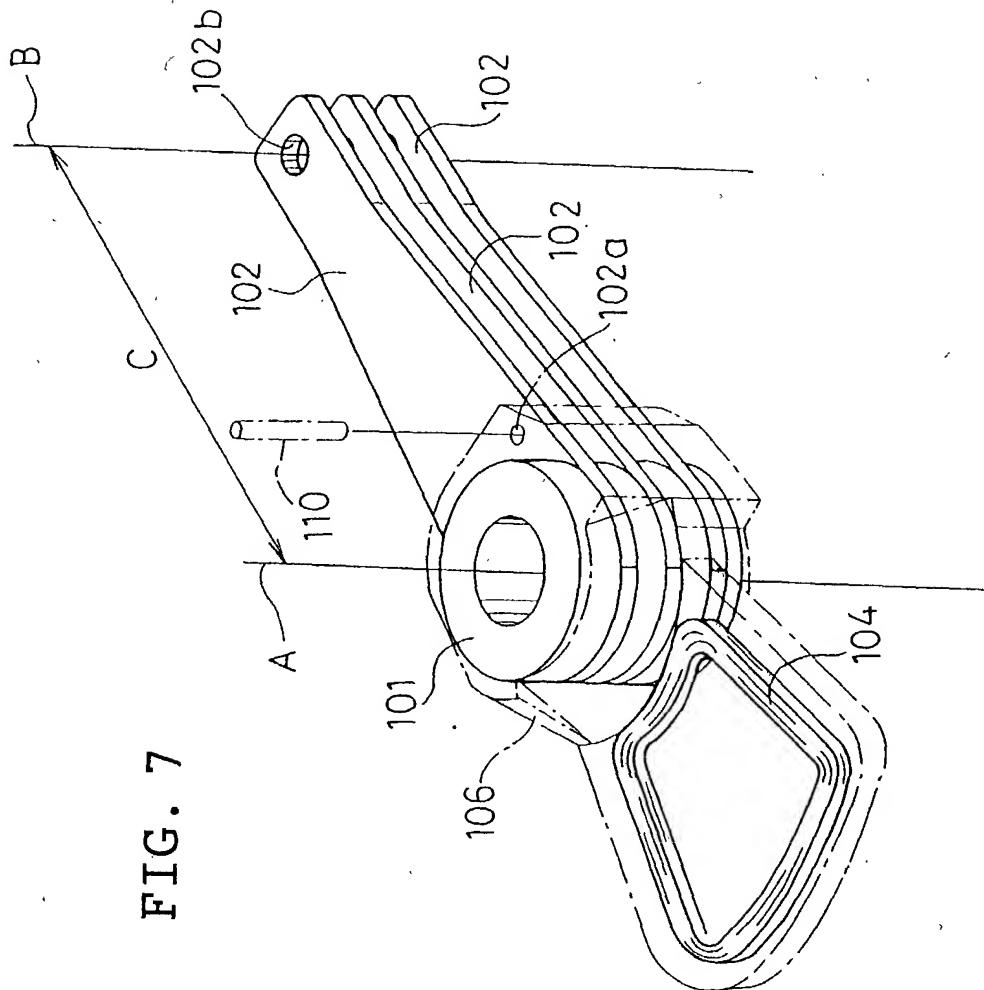


Figure 1 consists of two cross-sectional views, (a) and (b), of a semiconductor device. Both views show a central core 101, a top layer 102, and a bottom layer 104. The device is mounted on a substrate 107. In view (a), the top layer 102 is a single layer, and the bottom layer 104 is a single layer. In view (b), the top layer 102 is a multi-layered structure, and the bottom layer 104 is a multi-layered structure. The device is shown in a cross-sectional view, with the substrate 107 and the device layers 101, 102, and 104. The device is mounted on the substrate 107, and the layers 101, 102, and 104 are shown in cross-section. The device is shown in a cross-sectional view, with the substrate 107 and the device layers 101, 102, and 104. The device is mounted on the substrate 107, and the layers 101, 102, and 104 are shown in cross-section.